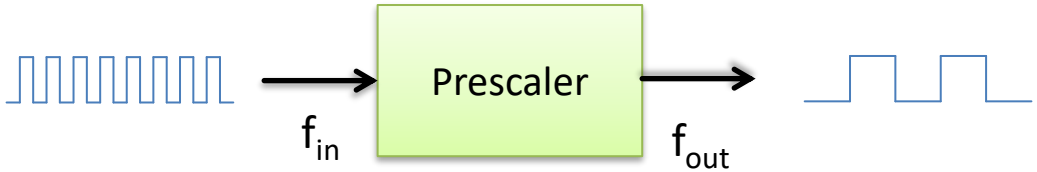
Prescalers

Digital Electronics

by Wolfgang Neff

Prescalers (1)

- Reduces the frequency of an input signal
  - Also called
    - Clock divider
    - Frequency divider
  - Divides the input frequency by a factor



$$f_{out} = \frac{f_{in}}{n}$$

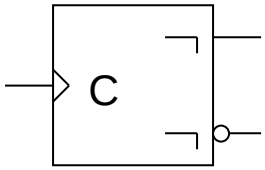
Prescalers (2)

- Frequency is Reduced by Counting
  - Example
    - Mod-8 counter → 3 binary digits (Q_0, Q_1, Q_2)

Ticks	0	1	2	3	4	5	6	7	Div
Clock	0 1 0 1	0 1 0 1	0 1 0 1	0 1 0 1	0 1 0 1	0 1 0 1	0 1 0 1	0 1 0 1	1
Q_0	0	1	0	1	0	1	0	1	2
Q_1	0	0	1	1	0	0	1	1	4
Q_2	0	0	0	0	1	1	1	1	8

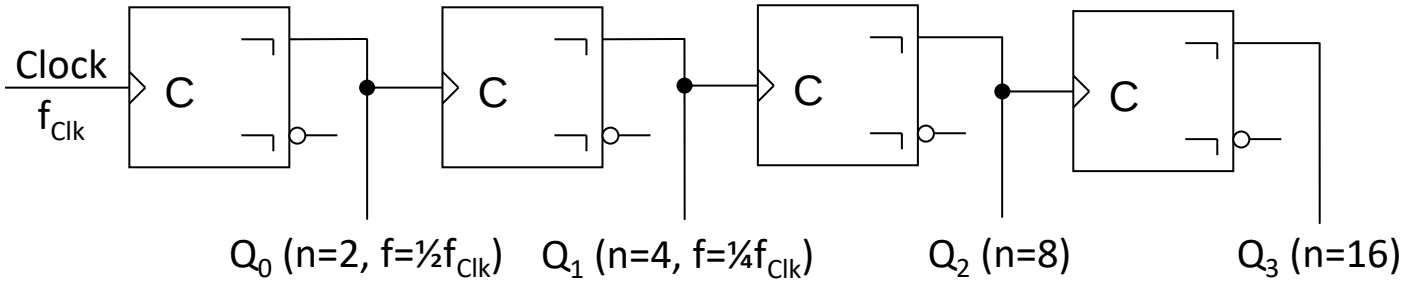
Prescalers (3)

- Implementation
  - Use T flip-flops (toggles its state)



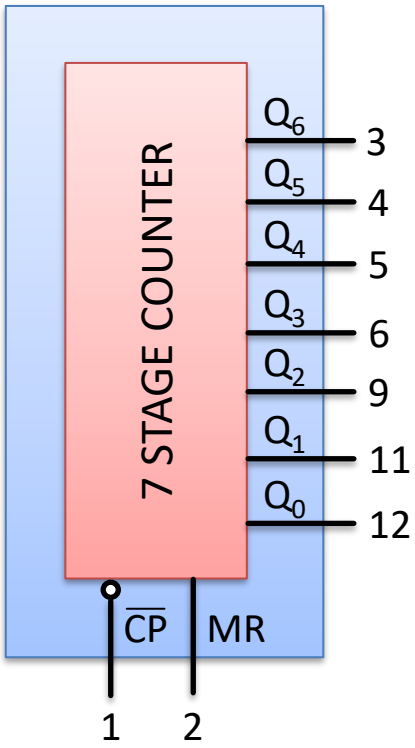
Q^+	Action
¬Q	Toggle state

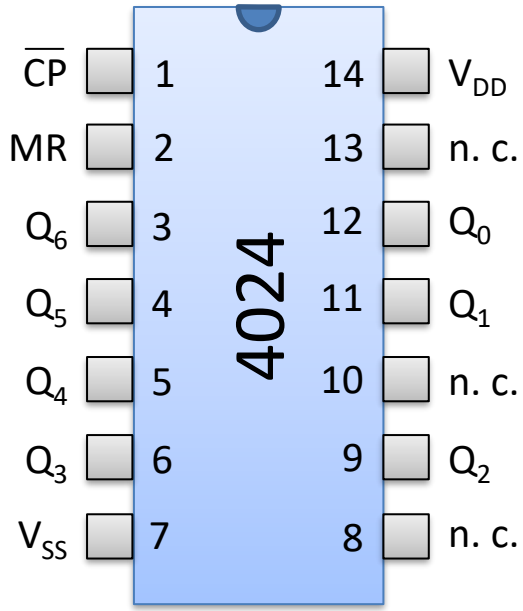
  - Cascade
    - Example: 4 stage frequency divider



Prescalers (4)

- 4024 – 7-stage frequency divider





Prescalers (5)

- 4024 – 7-stage frequency divider (continued)

Symbol	Pin	Description
$\overline{CP}$	1	clock input
MR	2	master reset input
V_{SS}	7	ground
n. c.	8, 10, 13	not connected
Q_0, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6	12, 11, 9, 6, 5, 4, 3	buffered parallel outputs
V_{DD}	14	supply voltage